REMARKS

New claims 108-121 have been added, and claims 1-107 have been cancelled. Accordingly, claims 108-121 remain pending.

The Examiner's objections and rejections under 35 U.S.C. §112, first paragraph, are considered moot in light of the new claims.

The new claims do not add any new matter and are described in the specification. Accordingly, it is respectfully submitted that the pending claims meet the requirements under 35 U.S.C. §112, first paragraph.

Claim 108 recites a "method of fabricating a semiconductor die." Claims 108 also recites "forming a test structure on the semiconductor die, wherein at least a portion of the test structure includes a dummy structure, wherein the test structure permits voltage contrast testing." This element is supported in the specification on page 43, last paragraph, among other places, which specifies "another test structure that may be formed within the intermediate section 210 of the test die 204 is the test structures using CMP dummy metal fillings as a test pad to test for vias." Also, Figures 9 and 26a-26c and their accompanying text on page 44 describe exemplary voltage contrast type test structures which include a dummy shape or structure. The test structure embodiments of Figure 9 are described specifically as having one or more stacked metal layers which are coupled to the substrate and a metal filler (or dummy filler or structure) on page 44, 2nd paragraph. The embodiments of Figure 26a-26c are described as including dummy structures which are coupled to the substrate through one or more contacts and other dummy structures which are left floating on page 44, last paragraph.

The Examiner has previously argued that the phrase "adding dummy filling within a top conductive layer of the plurality of conductive layers so as to minimize defects" is unclear. It is respectfully submitted that the formation of dummy structures, in general, is a well known technique. That is, the formation of dummy structures is well known to those skilled in the art. By way of example, several dummy structures and techniques for forming dummy structures are generally described in U.S. Patents 6,109,775 and 5,654,897.

Claim 108 also recites "performing voltage contrast testing on the test structure to detect electrical defects within the test structure." This element is supported in the specification on page 44, last paragraph, among other places, which recites that the exemplary test structures of

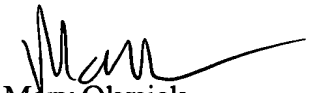
Figures 26a-26c are designed "to permit voltage contrast testing." Voltage contrast testing is also described in more general terms on page 44, 2nd paragraph, which describes how defects may be detected in the test structure of Figure 9 by determining whether electrons are emitted. For instance, on page 44, 2nd paragraph the specification recites:

> "If a defect free path to substrate is established, metal filler 900 emits secondary electrons, indicating that the [underlying] via and the contact are not open. If any one of them are open, the metal filler remains dark."

Exemplary structures for the embodiments of claims 109-120 are described with respect to Figures 9 and 26a-26c and their accompanying text as outlined above. Formation of another exemplary voltage contrast test structure coupled to a dummy structure is described on page 5, third paragraph, which recites formation of "a plurality of conductive layers and a test structure from at least one of the plurality of conductive layers" and that "dummy fillings are added within a top conductive layer of the plurality of conductive layers so as to minimize defects from CMP."

Applicants believe that all pending claims are allowable and respectfully requests a Notice of Allowance for this application from the Examiner. Should the Examiner believe that a telephone conference would expedite the prosecution of this application, the undersigned can be reached at the telephone number set out below.

Respectfully submitted,
BEYER WEAVER & THOMAS, LLP



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